Date: June 16, 2017

EIC Detector R&D Progress Report and Proposal

Project ID: eRD18
Project Name: Precision Central Silicon Tracking & Vertexing for the EIC
Period Reported: January 1 to June 16, 2017
Project Leader: Peter Jones
Contact Person: Peter Jones

Project Members: P.P. Allport, S. Bailey, L. Gonella, P.G. Jones[*], P.R. Newman
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Abstract

We propose to develop a detailed concept for a central silicon pixel detector for an Electron-Ion Collider at BNL or JLab exploring the advantages of using HV-CMOS or HR-CMOS MAPS technologies to achieve improved spatial resolution. The sensor development will exploit the newly created Birmingham Instrumentation Laboratory for Particle Physics and Applications. An accompanying simulation study will optimise the basic layout, location and sensor/pixel dimensions to find the best achievable momentum resolution and vertex reconstruction resolution. This initial design study will allow future full-detector simulations to explore precision measurements of heavy flavour processes and scattered electrons at high Q^2.

1. Report

1.1 What was planned for this period?

The work plan for the second half of FY17 was to complete test structure submissions as part of our ongoing work on a UK-funded Digital Electromagnetic Calorimeter R&D project (DECAL) and through our membership of the RD50 Collaboration (WP1 in the original proposal), and to begin work on detector layout simulations for the barrel silicon tracker (WP2 in the original proposal). In January we reported on a new opportunity to collaborate with CERN to test a demonstrator chip fabricated using a modified version of the TowerJazz process used for the ALPIDE (ALICE ITS) sensor. Of all the options currently available, the CERN demonstrator chip appears to be the most relevant given our current understanding of the requirements of a future EIC detector. The characterisation of the demonstrator chip will therefore be our main focus for the remainder of this period and FY18. Further justification will be given below.

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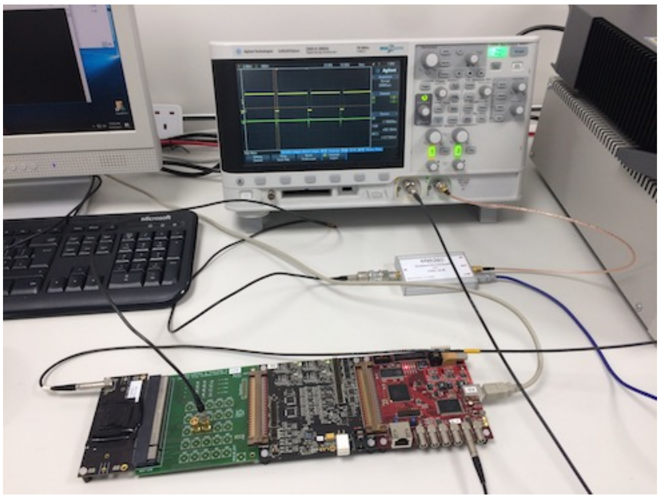
1.2 What was achieved?

WP1 – Sensor development

Perhaps the most significant development in the last 6 months is that we have been given access to a demonstrator chip developed by collaborators at CERN. The demonstrator uses a modified version of the HR-CMOS variant of the TowerJazz 180 nm process employed for the ALPIDE sensor [1]. In the modified process, a larger depletion region is achieved by the introduction of a planar junction in the epitaxial layer. The demonstrator chip contains more than 100 matrices of pixels with different sizes, size of collection electrode and spacing between the collection electrode and embedded electronics. It will permit a systematic study of charge collection as a function of pixel size and geometry and provides an excellent test vehicle for the EIC detector design studies outlined in our original proposal. This opportunity has arisen out of our involvement in other MAPS projects discussed below and makes EIC relevant pixel tests possible at an early stage of this project.

We now have a demonstrator chip in Birmingham and the readout system has been commissioned (see Fig. 1). While we hope to have some initial studies to show at the EIC R&D meeting in July, a comprehensive evaluation of the demonstrator chip forms a large part of our proposed work plan for the next 12 months.



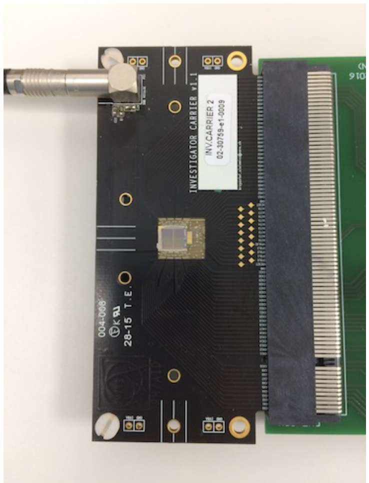


Figure 1. CERN demonstrator chip and readout card in Birmingham (left); the demonstrator chip revealed on its carrier card (right).

Test structures have also been submitted to the TowerJazz foundry as part of our ongoing DECAL MAPS development. The first submission will employ the standard 180 nm process used for the ALPIDE sensor, albeit with a larger pixel format, using multiple collection electrodes in each pixel in an attempt to improve charge collection by drift. A second submission employing the modified TowerJazz process used in the CERN demonstrator chip has also been made, again consisting of somewhat larger pixels ($40 \times 40\ \mu m^2$ and $50 \times 50\ \mu m^2$) with multiple collection electrodes. This second submission was part of a multi-project design wafer submitted with collaborators from CERN and the University of Bonn. Although possibly less relevant for this project, due to their larger pixel sizes in comparison to the ALPIDE sensor ($30 \times 30\ \mu m^2$), these structures will validate the use of multiple electrodes in a pixel to improve charge collection by drift. It is important to note that constraints on the pixel size are driven by a project with different requirements to the application being proposed here.

Prototype pixel matrices and test structures are also currently being prepared for a submission with LFoundry. This work is being undertaken by the RD50 collaboration [2]. Submission has been delayed with respect to our original timetable and is now expected to happen toward the end of the year. Designers are currently working on matrices with improved time resolution, different pixel formats and options to test the possible stitching of sensors. In addition, test structures will permit the study of the charge collection properties of pixels down to 20 x 20 μm^2, a size that is potentially more relevant for the EIC inner tracker.

WP2 – Detector layout simulations

EIC R&D funds provided support for Dr. Sam Bailey, a junior postdoctoral researcher, in FY17. The post was filled at the beginning of March 2017, so we have had 3 months of PDRA support so far in this funding period. The initial plan was to gain familiarity with EIC-ROOT and to make connections with some of the physics performance plots in the EIC White Paper and with ongoing simulations by the LBNL group in eRD16. With the help of Alexander Kiselev, the EIC-ROOT framework is now up and running in Birmingham. A few bugs and other software issues have been discovered in this process. These are now mostly resolved and the fixes have been propagated back to the master version. We are now at a stage where we can perform momentum resolution and impact parameter studies for a standalone central silicon barrel.

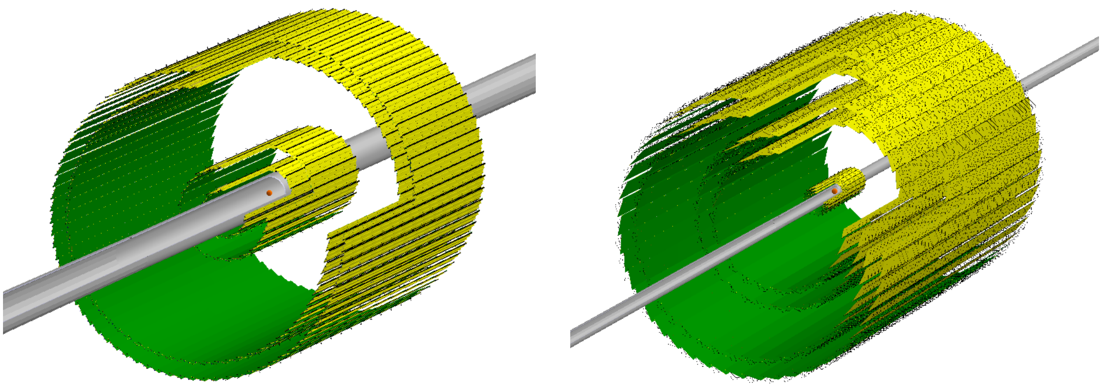


Figure 2. Default 4-layer barrel (left); ALICE ITS-like 7-layer barrel (right).

Fig. 2 shows two central silicon barrel designs used as a starting point for the detector layout simulations. The design shown in the left panel of Fig. 2 is the default configuration in EIC-ROOT, which is a 4-layer barrel with an inner and outer radius of 23.4 mm and 157.2 mm, respectively. The design shown in the right panel is similar to the ALICE ITS, which is a 7-layer barrel with an inner and outer radius of 23.4 mm and 395 mm, respectively.

The aim of these initial studies was simply to check that the simulation framework is producing sensible results before carrying out a more careful, systematic study. We also wanted to make a connection with the simulations of eRD16 that were shown in January. In those simulations, the relative momentum resolutions of electrons at four different energies were presented as a function of pseudorapidity assuming a 1.5 Tesla magnetic field [3]. Fig. 3 shows the results for the default 4-layer barrel and ALICE ITS-like 7-layer barrel in the pseudorapidity interval $|\eta| < 1$. We note that the electron momenta are chosen to match earlier simulations. The relative momentum resolution of the 4-layer detector is significantly worse that the 7-layer design. The difference comes mainly from the reduced radial size of the 4-layer detector. This was checked by simulating an expanded 4-layer detector, not shown here, which gave similar results to the 7-layer design. In all cases, the relative momentum resolution is that of a standalone barrel and does not include an outer tracker. Once again, this was chosen to allow comparison with the simulations of eRD16. Our results for the 7-layer design are in reasonably close agreement with those simulations, which also considered an ALICE ITS-like design in the central region, but also incorporating forward and backward disks.

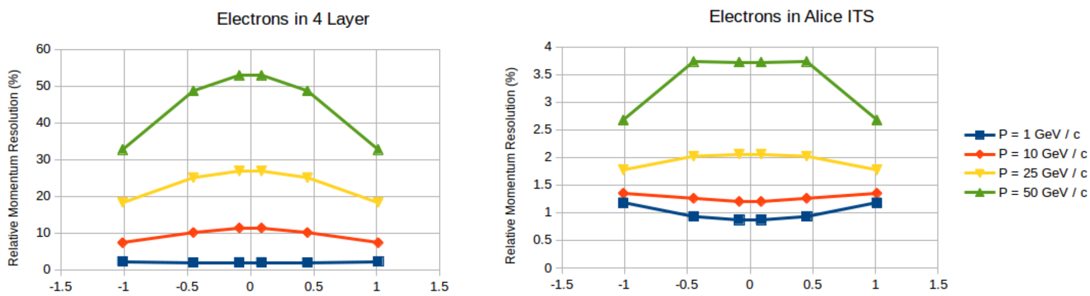


Figure 3. Relative momentum resolution (%) as a function of pseudorapidity for electrons at four different energies. Default 4 layer barrel (left); ALICE ITS-like 7 layer barrel (right).

A first look at impact parameter resolution is shown in Fig. 4. Shown here is the *rms* 3-d distance of closest approach of electrons to the primary vertex. The results of the compact 4-layer design and the larger 7-layer design are similar, indicating that the proximity of the first layer to the IP and the intrinsic spatial resolution of the detector are driving factors. The position resolution for 1 GeV/c electrons is slightly worse in the case of the ALICE ITS-like 7-layer design, presumably due to the increased effect of multiple scattering in the presence of more layers. The position resolution is slightly improved in the expanded 4-layer design at all momenta compared to the default compact design.

For the July meeting, we hope to have made similar studies for pions over a physically meaningful range of momenta, with and without the additional lever arm provided by the outer TPC tracker.

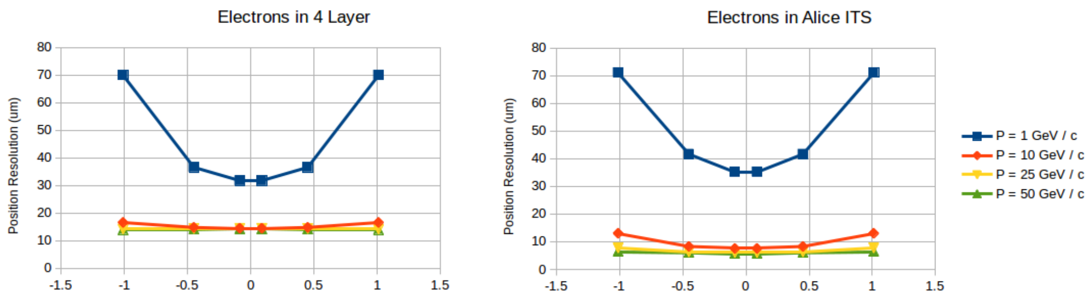


Figure 4. Impact parameter resolution (μm) as a function of pseudorapidity for electrons at four different energies. Default 4 layer barrel (left); ALICE ITS-like 7 layer barrel (right).

1.3 What was not achieved, why not, and what will be done to correct?

We believe that the project is on track at this stage. Although the RD50 submission has been delayed, these developments have to some extent been superseded by the availability of the CERN demonstrator chip. By the end of FY17 we will have started to characterise the demonstrator chip and will have performed an initial design performance study of the central barrel in terms of momentum resolution and impact parameter resolution as a function of the number and spacing of detector layers and the anticipated hit resolution.

1.4 What is planned for the next funding cycle and beyond? How, if at all, is this planning different from the original plan?

The answer to this question is covered in the Proposal section below.

1.5 What are critical issues?

Although not necessarily a critical issue, an important factor that needs to be addressed is timing. The potential advantages of HV/HR CMOS and modern lithographic processes are faster charge collection by drift and smaller feature sizes (smaller pixels). The optimal spatial resolution of the inner tracking system can be studied with existing simulation tools. The timing performance of the device will be determined by the charge integration time in-pixel. This must meet the requirements determined by the collision frequency of the machine, the anticipated beam luminosity and the interaction cross section.

2. Proposal

2.1 Introduction

Our proposal for the next funding period (FY18) builds upon our original proposal and focuses on the design of a precision central silicon tracking and vertex detector for a future EIC detector. The relevance for the EIC is high precision tracking and the identification of secondary vertices in the central region. As such, the requirements for the detector are likely to be driven by the reconstruction of displaced vertices from the decay of charmed and beauty hadrons. The focus of the EIC physics programme on the role of gluons in the structure of hadrons places a strong emphasis on heavy flavour observables. Heavy flavour production is directly sensitive to the gluon density in the hadron beam at lowest order as well as probing a wide range of issues in perturbative QCD. Similarly, the use of heavy flavours as probes of deconfinement in relativistic heavy-ion collisions provides further motivation to study the same observables in e+A collisions, where cold nuclear matter effects can be explored. Open charm production in polarised e+p scattering has also provided insight into the role of gluons in determining the spin structure of the proton. These points are fully recognised in the EIC White Paper [4] but there is no detailed study to date which looks closely at the optimization of the central silicon tracker layout to address this physics.

2.2 Proposed programme of work

At the January meeting, the Panel encouraged closer collaboration with eRD16, looking at forward/backward tracking. There are clear synergies between the two projects. eRD16 has already shown that there are some interesting and potentially important integration and performance issues relating to the interface between the barrel and the first planes of disks, closest to the IP. In the intervening period, we have exchanged several emails and had two face-to-face meetings over Skype that have proved to be very productive. It is clear that the performance of the barrel should not be studied in isolation of the forward/backward disks and a unified approach is desirable. Our starting point will therefore be to work on the layout simulations together, sharing the same geometry descriptions. We will then look at detector performance from the perspective of different physics observables. The emphasis of this proposal is on displaced vertices from heavy flavour hadron decays. At low and high x, heavy flavour production will be in the forward/backward regions, underlining the need for a unified approach. We will therefore continue to work with eRD16 to iterate towards a final inner silicon detector design incorporating both the barrel and the forward/backward disks. We will also collaborate on defining the sensor requirements, which may be somewhat different in the forward/backward and central regions. This proposal has an emphasis on sensor R&D and will seek to define the capability of the technology to meet the requirements coming from the simulations.

Our proposed programme of work for the next period is divided into two work packages: WP1 on sensor development and WP2 on detector layout investigations.

2.2.1 WP1: Sensor development

The technology solution we propose is based on Monolithic Active Pixel Sensors (MAPS). We aim to explore the latest developments in HV/HR-CMOS sensors and novel structures, such as multiple collection electrodes, to improve charge collection through drift rather than by diffusion. This promises to result in faster signals as well as reduced charge spreading and better signal-to-noise, ultimately leading to improved spatial resolution.

This work package will focus on evaluating test structures as they become available from different foundry processes benefiting from our involvement in other projects involving MAPS. As the CERN demonstrator chip fabricated using the TowerJazz modified process is already available, we will focus our efforts on characterising this device in the next funding period. We aim to complement the studies already undertaken by colleagues at CERN with eTCT and source measurements before and after irradiations [1]. We will measure charge collection efficiency, collection time and the width of the depletion region. It might be possible to test the chip in a test beam in collaboration with CERN. This would allow a study of in-pixel efficiency and cluster size, but will depend on the progress made with lab testing and time constraints within the project. As highlighted in the report section, we also expect to receive test structures that will allow us to study pixels with multiple collection electrodes fabricated in the TowerJazz standard and modified processes, and pixel matrices and test structures fabricated using the LFoundry process.

We plan, in parallel, to perform TCAD simulations with input from the simulations being carried out at Birmingham and LBNL to optimise the pixel layout and sensor thickness. TCAD simulations will also be used to optimise the number and spacing of guard rings around the pixel to minimise the inactive area at the edges of the sensor. This is necessary to minimise the amount of sensor overlap needed to obtain full azimuthal (barrel) and forward-angle (disks) coverage. The geometry of the forward/backward disks may prove to be particularly challenging from the point of view of minimising the overlap of detector layers and is an area we have identified where close collaboration with eRD16 would be beneficial.

2.2.2 WP2: Detector layout investigations

This work package is concerned with defining the requirements for the central silicon detector at a future EIC. Simulations are currently being performed using the BeAST detector concept developed by the BNL EIC Taskforce, but consideration will be given to both the JLab and BNL machine and detector options.

The starting point for simulations will be the shared geometry descriptions being developed jointly with eRD16. Rather than dividing tasks purely by whether they pertain to the central tracker or the forward/backward regions, we will each focus on different physics observables. This proposal is particularly concerned with open heavy flavour and the reconstruction of displaced vertices.

We propose to generate a sample of e+p events producing heavy flavour mesons to study the transverse momentum and rapidity of the decay daughters. This will be used to inform the range of momenta to be used in the detector layout simulations. Single hadrons will then be generated from the nominal IP with a physically meaningful range of momenta to simulate the decay daughters. This will permit momentum resolution and impact parameter studies without the need of formally identifying a secondary vertex. This is left to a later stage of the project.

We will consider the optimal layout of the inner tracking system in terms of the number of detector layers, their spacing, thickness and intrinsic spatial resolution. Of particular interest will be the standalone tracking capability at low transverse momenta and the combined performance of the inner silicon and outer TPC tracking system at higher momenta. Consideration will also be given to the matching of tracks reconstructed in the inner and outer tracking detectors, hence the optimal radius of the outermost silicon barrel layer.

The specific questions we wish to address are:

- How many layers are needed and at what radii?
- What is the optimal length of the barrel layers and what overlap in acceptance with the forward disks is possible/desirable?
- Assuming 0.3% radiation length per layer (0.8% for the outer layers), what is the optimal pixel size (resolution) and how does this vary with the layer thickness? What gains are to be had if multiple scattering can be reduced?

2.3 Request for resources

Wherever possible existing resources will be devoted to the project. This includes academic time (see Personnel), computing resources and consumables. It also includes access to test structures from submissions related to other projects. As mentioned in our initial proposal, the School of Physics has committed funds to support a 3.5-year PhD studentship to the project. We are pleased to report that this studentship has been taken up by Håkan Wennlöf from Sweden, who will start working on the project from October.

In FY17 we benefitted greatly from EIC R&D funds that supported Dr. Sam Bailey, a junior PDRA, at 0.5 FTE. This provided the impetus needed to start on the simulation work package. Good progress has been made in the 3 months that Bailey has been in post. Although we have a PhD student starting in October, they will have to attend classes for the first 6 months of their studies and it will take some time for them to come up to speed with the simulation framework. We also want the PhD student to work on testing the CERN demonstrator chip. Continued support of a PDRA in FY18 is therefore essential to enable us to define the requirements of the inner silicon tracking system in tandem with eRD16. As outlined below under External Funding, we have tried to find matching funding for the 0.5 FTE that we received this fiscal year. Sadly, this has not been forthcoming. We are therefore requesting support for a full-time PDRA for one year (1 FTE). This will permit a transfer of knowledge enabling the PhD student to make quicker progress as well as allowing us to meet the aims of this proposal. In addition, we are requesting travel support for Jones, Gonella, Bailey and the new PhD student to facilitate their participation in EIC R&D meetings. The costs are detailed below:

1. PDRA (1 FTE)	£107,394	\$150,351
2. Travel (4 x 2 x £1,250)	£10,000	\$14,000
Total		\$164,351

The requested amount (\$164k) represents the optimal level of funding. The travel component represents 8.5% of the requested amount. Descope options of -20% and -40% will inevitably impact the duration of the PDRA post, which would limit progress being made on the detector layout simulations. In this scenario, we would choose to prioritise the travel component over lengthening the duration of the PDRA post. The justification is that the PDRA and the PhD student have no alternative source of travel funding and travel support will help to facilitate collaboration, particularly with eRD16, as the project develops.

3. Personnel

Include a list of the existing personnel and what approximate fraction each has spent on the project. If students and/or postdocs were funded through the R&D, please state where they were located and who supervised their work.

Prof. Peter Jones (0.05 FTE) – no cost to project
Dr. Laura Gonella (0.2 FTE) – no cost to project
Dr. Sam Bailey – (0.5 FTE) – supported by EIC R&D funds in FY17
Prof. Phil Allport and Prof. Paul Newman have an advisory role and participate in our regular project meetings to monitor progress.

4. External Funding

Describe what external funding was obtained, if any. The report must clarify what has been accomplished with the EIC R&D funds and what came as a contribution from potential collaborators.

In FY17, EIC R&D funds supported a junior postdoctoral researcher at 0.5 FTE. We applied for matching funds as part of our 4-year Nuclear Physics Consolidated Grant bid. However, we have just heard that no new posts were awarded. Sadly, due to budgetary constraints, there was no opportunity to bid for UK R&D funds through the STFC Project Research and Development (PRD) scheme this year. There may be a future call for R&D projects in 2018.

5. Publications

Please provide a list of publications coming out of the R&D effort.

Not applicable at this stage of the project.

References

[1] H. Pernegger et al., First tests of a novel radiation hard CMOS sensor process for Depleted Monolithic Active Pixel Sensors, 2017 JINST 12 P06008.

[2] E. Vilella-Figueras, Recent progress of the RD50 collaboration towards an R&D HV-CMOS submission in the 150 nm node from LFoundry, 30th RD50 workshop, Krakow, June 2017.

[3] E. Sichtermann et al., eRD16: Forward/Backward Tracking at EIC using MAPS Detectors (slide 19), EIC Generic Detector R&D Advisory Committee Meeting, Brookhaven National Laboratory, January 2017.
https://wiki.bnl.gov/conferences/images/6/6e/EIC-eRD16-Sichtermann.pdf

[4] A. Accardi et al., (EIC White Paper), Electron Ion Collider: The Next QCD Frontier, Understanding the glue that binds us all, Eur. Phys. J. A (2016) 52:268